AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

19. (currently amended): An information processing apparatus comprising:

a first computer module which includes a first controller and a second computer module which includes ~~another~~ a second controller, wherein:

~~said each of said first and second computer modules includes a processor, a first memory, and a second memory~~

said first computer module includes a first processor, a first main-memory and a first sub-memory;

said second computer module includes a second processor, a second main-memory and a second sub-memory;

said first ~~processors~~processor and said second processor operate ~~execute the same instructions~~ substantially simultaneously and are substantially synchronized with each other;

~~said each first memory is read and written by the processor which is on the same computer module~~

said first controller writes data to said first main-memory and said second sub-memory according to a first write request of said first processor, and at the substantially same time, said second controller writes data to said second main-memory and said first sub-memory according to a second write request of said second processor;

wherein said first and second write requests are associated with the same data.~~;~~

~~said each second memory is read and written by the processor which is on the same computer module and is written by said processor which is on the other computer module;~~

~~wherein data is written to the first memory of the first computer module and the same data is written to at least the second memory of the first computer module; and~~

~~wherein, during a normal process, said first processor works by means of said first memory which is on the first computer module and said second memory is written by said processor which is on the second computer module, and wherein, during a rejoining process, said first processor switches from working by means of said first memory which is on the first computer module to working by means of said second memory which is on the first computer module.~~

20. (currently amended): The information processing apparatus as claimed in claim 19, wherein said ~~each~~ first controller controls so that ~~during the normal process~~while said first processor and said second processor are synchronized, read access from said first processor ~~which is on the same computer module~~ is carried out as against said first main-memory ~~which is on the same computer module~~ and write access from said first processor ~~which is on the same computer module~~ is carried out as against said first main-memory and said second ~~memories~~ sub-memory ~~which are on the same computer module~~ and write access from said second processor ~~which is on the other computer module~~ is carried out as against said ~~second~~ first sub-memory ~~which is on the same computer module~~, and said first ~~each~~ controller controls so that, ~~during the rejoining process~~when said first processor fails to be in synchronism with said second

processor, read access from said first processor ~~which is on the same computer module~~ is carried out as against said ~~second~~ first sub-memory ~~which is on the same computer module~~ and write access from said first processor ~~which is on the same computer module~~ is carried out as against ~~said first and said second memory which are on the same computer module and said second memory which is on the other computer module~~said first main-memory, said first sub-memory and said second sub-memory.

21. (currently amended): The information processing apparatus as claimed in claim 20, wherein said ~~each~~ first controller copies the contents of said ~~second~~ first sub-memory ~~which is on the same computer module~~ to said first main-memory ~~element which is on the same computer module~~ when ~~no read or write access from said processor which is on the same computer module to said second memory is present during the rejoining process~~said first processor fails to be in synchronism with said second processor.

22. (currently amended): The information processing apparatus as claimed in claim 21, wherein said ~~each~~ first controller copies the contents of said ~~second~~ first sub-memory to said first main-memory by means of a direct memory access circuit.

23. (currently amended): The information processing apparatus as claimed in claim 21, wherein ~~a state of~~ said first processor ~~computer module~~ recovers said synchronism with said second processor ~~changes to the normal state from the rejoining state~~ when said~~the~~ copy is completed for all memory areas of said ~~second~~ first sub- memory.

24. (currently amended): The information processing apparatus as claimed in claim 22, wherein ~~a state of~~ said first processor ~~computer module~~ recovers said synchronism with said second processor ~~changes to a normal state from the rejoining state~~ when the copying is completed for all memory areas of said ~~second~~ first sub-memory.

25. (currently amended): The information processing apparatus as claimed in claim 19, wherein said first and second controllers are connected as a ring for three or more ~~said~~ another computer modules.

26. (currently amended): The information processing apparatus as claimed in claim 20, wherein said first and second controllers arc connected as a ring for three or more ~~said~~ another computer modules.

27. (currently amended): The information processing apparatus as claimed in claim 21, wherein said first and second controllers are connected as a ring for three or more ~~said~~ another computer modules.

28. (currently amended): The information processing apparatus as claimed in claim 22, wherein said first and second controllers are connected as a ring for three or more ~~said~~ another computer modules.

29. (currently amended): The information processing apparatus as claimed in claim 23, wherein said first and second controllers are connected as a ring for three or more ~~said~~ another computer modules.

30. (currently amended): The information processing apparatus as claimed in claim 24, wherein said first and second controllers are connected as a ring for three or more ~~said~~ another computer modules.

31. (previously presented): The information processing apparatus as claimed in claim 19, wherein said first and second computer modules are on lockstep fault tolerant computer system.

32. (previously presented): The information processing apparatus as claimed in claim 20, wherein said first and second computer modules are on lockstep fault tolerant computer system.

33. (previously presented): The information processing apparatus as claimed in claim 21, wherein said first and second computer modules are on lockstep fault tolerant computer system.

34. (previously presented): The information processing apparatus as claimed in claim 22, wherein said first and second computer modules are on lockstep fault tolerant computer system.

35. (previously presented): The information processing apparatus as claimed in claim 24, wherein said first and second computer modules are on lockstep fault tolerant computer system.

36. (previously presented): The information processing apparatus as claimed in claim 30, wherein said first and second computer modules are on lockstep fault tolerant computer system.

37. (canceled)